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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,335	11/19/2003	Joichi Bita	3408.68745	8257

7590 02/13/2007

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EXAMINER	
DILLON, SAMUEL A	
ART UNIT	PAPER NUMBER
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/717,335	BITA ET AL.	
	Examiner	Art Unit	
	Sam Dillon	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-17* is/are rejected.

7)☒ Claim(s) *2 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 25, 2007 has been entered. Per the amendment, Claim 17 has been added.

2. The instant application having Application No. 10/717,335 has a total of 17 claims pending in the application; there are 3 independent claims and 14 dependent claims, all of which are ready for examination by the examiner.

I. RESPONSE TO AMENDMENT(S) / ARGUMENT(S)

3. Applicant's arguments *(page 12 lines 3-19)* with respect to the 35 U.S.C. 103(a) rejections of Claims 1-16 have been fully considered and are **persuasive**, but regarding Claims 1, 3-9 and 11-16 are moot in view of the new ground(s) of rejection, as described below. The rejections of Claims 2 and 10 are withdrawn. However, the Examiner notes that Hubis does disclose several features that the Applicant contends it does not.

4. The Applicant contends that Hubis does not disclose **a first controller acquiring a storage page in the mirror area of the cache memory of a second controller by referring to a mirror management table in the first controller**. Though Hubis was not relied upon for this feature in previous rejections, the Examiner respectfully disagrees.

Hubis discloses that one controller forwards a write operation to another controller's mirror area via a special write command *(column 3 lines 47-63)*. This process culminates in the creation of a new cache entry in the other controllers mirror cache, and

can be interpreted as a process that acquires a storage page in the mirror area of the cache memory.

The write command includes a write program *(column 3 lines 34-35)*, which is inherently a listing of instructions. This listing of instructions can be considered a table of instructions *("a systematic arrangement of data", www.m-w.com/dictionary/table)*. It can additionally be considered a mirror management table, in that it is a table of instructions that when executed manages *(causes)* the mirroring operation between caches.

Finally, the first controller executes the write command by referring to the write command's program listing. Accordingly, Hubis does disclose a first controller *(controller 1, figure 2)* acquiring a storage page *(cache entry)* in the mirror area *(write mirror cache 118-2, figure 2)* of the cache memory of a second controller *(controller 2, figure 2)* by referring to a mirror management table in the first controller *(first controller refers to the program listing of the write command)*.

5. The Applicant contends that Hubis does not disclose **one controller managing a paging allocation of a mirror area in the other controller**. The Examiner respectfully disagrees.

As stated above, Hubis discloses one controller *(controller 1, figure 2)* managing *(the controller initiates a process that cause the action to happen)* a paging allocation *(creation of a cache entry)* of a mirror area *(write mirror cache 118-2, figure 2)* in the other controller *(controller 2, figure 2)*.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102 - Hubis

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 1, 4, 7, 9, 12, 15 and 17** are rejected under 35 U.S.C. 102(b) as being anticipated by Hubis *(US Patent Number 6,321,298)*.

8. As per **Claim 1**, Hubis discloses a storage control apparatus *(figure 1)* for accessing a storage device *(shared storage devices 108)* according to a data access request *(host write command 128, column 3 lines 49-50)* from a requesting apparatus *(host computer 1, figure 1)*, comprising:

a first controller *(RAID controller 1, figure 1)* which has a first cache memory *(cache 112-1, figure 1)* and is in charge *(via bus 110, figure 1, see below)* of a first storage device *(any of shared storage devices 108)* out of a plurality of storage devices *(shared storage devices 108)*; and

a second controller *(RAID controller 2)* which has a second cache memory *(cache 112-2, figure 1)* and is in charge *(via bus 110, figure 1, see below)* of a second storage device *(any of shared storage devices 108)* out of said plurality of storage devices, and

a mirror area *(write mirror cache 118-2, figure 2)* of said second cache memory, and a mirror area *(write mirror cache 118-1, figure 2)* of said first cache memory,

said first controller further comprises a first management table *(write program listing, column 3 lines 34-35)* for managing allocation of a storage page

(cache entry) in a mirror area *(write mirror cache 118-2, figure 2)* of said second cache memory, and said second controller further comprises a second mirror management table *(respective write program listing, column 3 lines 34-35)* for managing allocation of a storage page in a mirror area *(write mirror cache 118-1, figure 2)* of said first cache memory

and wherein when said first controller receives a data write request *(host write command 128, column 3 lines 49-50)* containing write data from said requesting apparatus, said first controller allocates a page *(destination in first controller, see below)* in a read/write area *(write cache 116-1, figure 2)* of said first cache memory, acquires a storage page *(subset of mirror area, see below)* in the mirror area of said second cache memory by referring to said first mirror management table *(executes the write program, column 3 lines 34-35)*, writes *(transfer 107-1, figure 2)* the write data *(write data 138, column 3 line 51)* from said requesting apparatus to the page allocated in the read/write area of said first cache memory, and copies *(column 3 lines 55-58)* the write data to the acquired page in the mirror area of said second cache memory.

The Examiner notes that inherent in writing data to the read/write area in the first controller is the data being written to a subset of the read/write area, where a subset is either the entirety or a part of the read/write area. Subsequently, this subset fulfills the limitation *"a page in a read/write area"* cited on page 23 line 19. It is also inherent in copying the data to the mirror area of the second controller that the data is written to a subset of the mirror area, and this subset fulfills the limitation *"a storage page in the mirror area"* cited on page 23 line 20.

9. As per **Claim 4**, Hubis discloses the storage control apparatus according to Claim 1, wherein

when said first controller is degraded *(Hubis, "failure of controller", column 1 lines 38-41)*, said second controller takes charge of the storage apparatus which said first controller is in charge of *(Hubis, column 1 lines 45-48)*, and links the copy page in the mirror area of said second cache memory to said read/write area *(Hubis, column 1 lines 45-48)*.

10. As per **Claim 7**, Hubis disclose the storage control apparatus according to Claim 1, wherein each one of said first and second controllers comprises:

a control unit *(Hubis, processor 200, figure 3)* for controlling said cache memory and said storage device; and

a node channel circuit *(Hubis, backend disk bus 110, figure 3)* for performing direct communication between said control units.

11. As per **Claim 9**, Hubis discloses a storage control method for accessing a storage device *(Hubis, shared storage devices 108)* according to a data access request *(Hubis, host write command 128, column 3 lines 49-50)* containing write data from a requesting apparatus *(Hubis, host computer 1, figure 1)*, comprising the steps of:

allocating a page *(Hubis, subset of read/write area, see rejection of claim 1)* in a read/write area *(Hubis, write cache 116-1, figure 2)* of a first cache memory *(Hubis, cache 112-1, figure 1)* disposed in one controller *(Hubis, RAID controller 1, figure 1)* of a pair of controllers *(Hubis, RAID controllers 1 and 2, figure 1)* when said one controller receives a data write request *(Hubis, host write command 128, column 3 lines 49-50)* from said requesting apparatus;

acquiring a storage page *(Hubis, subset of mirror area, see rejection of claim 1)* in a mirror area *(Hubis, write mirror cache 118-2, figure 2)* of a second

cache memory *(Hubis, cache 112-2, figure 1)* referring to a first mirror management table *(Hubis, write program, column 3 lines 34-35)* which is disposed in said one controller for managing allocation of a storage page in the mirror area of said second cache memory of said other controller;

writing *(Hubis, transfer 107-1, figure 2)* the write data *(Hubis, write data 138, column 3 line 51)* from said requesting apparatus to the page allocated in the read/write area of said first cache memory; and

copying *(Hubis, column 3 lines 55-58)* the write data to the acquired page in the mirror area of said second cache memory after said writing.

12. As per **Claim 12**, Hubis discloses the storage control method according to Claim 9, further comprising

a step of taking charge *(Hubis, column 1 lines 45-48)* of the storage device which said one controller is in charge of by said other controller when said one controller is degraded *(Hubis, "failure of controller", column 1 lines 38-41)*, and linking the storage page in the mirror area of said second cache memory to the read/write area of the second cache memory *(Hubis, column 1 lines 45-48)*.

13. As per **Claim 15**, Hubis discloses the storage control method according to Claim 9, wherein each one of said pair of controllers comprises

a control unit *(Hubis, processor 200, figure 3)* for controlling said cache memory and said storage apparatus, and

a node channel circuit *(Hubis, backend disk bus 110, figure 3)* for performing direct communication between said control units.

14. As per **Claim 17**, Hubis discloses a storage control apparatus for accessing a storage device according to a data access request from a requesting apparatus, comprising:

a first controller *(RAID controller 1, figure 1)* which has a first cache memory *(cache 112-1, figure 1)* and is in charge *(via bus 110, figure 1, see below)* of a first storage device *(any of shared storage devices 108)* out of a plurality of storage devices *(shared storage devices 108)*; and

a second controller *(RAID controller 2)* which has a second cache memory *(cache 112-2, figure 1)* and is in charge *(via bus 110, figure 1, see below)* of a second storage device *(any of shared storage devices 108)* out of said plurality of storage devices, wherein

said first controller further comprises a first mirror management table *(respective write command program listing, column 3 lines 34-35)* for managing allocation of a storage page *(cache entry)* in a mirror area *(write mirror cache 118-2, figure 2)* of said second cache memory, and said second controller further comprises a second mirror management table *(respective write command program listing, column 3 lines 34-35)* for managing allocation of a storage page in a mirror area *(write mirror cache 118-1, figure 2)* of said first cache memory,

wherein when said first controller receives a data write request *(host write command 128, column 3 lines 49-50)* containing write data from said requesting apparatus, said first controller allocates a page *(destination in first controller, see below)* in a read/write area *(write cache 116-1, figure 2)* of said first cache memory, acquires a storage page *(subset of mirror area, see below)* in the mirror area of said second cache memory by referring to said first mirror management table *(executes the write program, column 3 lines 34-35)*, writes *(transfer 107-1, figure 2)* the write data *(write data 138, column 3 line 51)* from said requesting apparatus to the page allocated in the read/write area of said first cache memory,

and copies *(column 3 lines 55-58)* the write data to the acquired page in the mirror area of said second cache memory, and

wherein one of said first and second controller manages a paging allocation of a mirror area in the other of said first and second controller *(each controller manages a write operation that results in the creation of a cache entry, a page per se, column 3 lines 34-60)*.

Claim Rejections - 35 USC ' 103 – Hubis and Tam

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. **Claims 3 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis *(US Patent Number 6,321,298)* and in view of Tam et al. *("A Taxonomy-Based Comparison of Several Distributed Shared Memory Systems")*.

17. As per **Claim 3**, Hubis discloses the storage control apparatus according to claim 1, wherein said first controller writes *(Hubis, column 3 lines 50-51)* back the data, which is written in the page allocated in the read/write area of said first cache memory *(Hubis, column 3 lines 50-52)*, to said storage device. Hubis does not disclose the storage control apparatus then releasing said acquired page of said first mirror management table.

Tam discloses releasing *("pass back the page", section 2.1.3, lines 8-9)* said acquired page *(page, section 2 paragraph 3 line 1)* of said first mirror management table.

Hubis and Tam are analogous art in that they deal with maintaining coherency in shared memory systems. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the write procedure between caches of Hubis lock the pages they access, as per the teachings of Tam.

The motivation for doing so would have been making sure the caches are synchronized, something Hubis is concerned with *(column 1 lines 49-51)*. Tam discloses that a cache coherence protocol is needed to ensure that caches always read a valid copy of a page *(section 1.2, line 11-12)*. Therefore, it would have been obvious to combine Hubis's caches with Tam's cache coherence protocol for the benefit of ensuring caches always read valid copies of pages to obtain the invention as specified in claim 3.

18. As per **Claim 11**, Hubis and Tam disclose the storage control method according to claim 9, further comprising the steps of:

writing back *(Hubis, column 3 lines 50-51)* the data, which is written in the page allocated in the read/write area of said first cache memory *(Hubis, column 3 lines 50-52)*, to said storage device; and

releasing *(Tam, "pass back the page", section 2.1.3, lines 8-9)* said acquired page *(Tam, page, section 2 paragraph 3 line 1)* of said first mirror management table when said write back completes.

Claim Rejections - 35 USC ' 103 – Hubis and Beardsley

19. **Claims 5 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis *(US Patent Number 6,321,298)* and in view of Beardsley et al. *(US Patent Number 6,304,980)*.

20. As per **Claim 5**, Hubis discloses the storage control apparatus according to Claim 4, but does do not disclose wherein said second controller disables read/write processing to the mirror area of said second cache memory.

Beardsley discloses said second controller disabling *(step 945, figure 9)* read/write processing to the mirror area of said second cache memory.

The primary controller in Hubis accesses *(column 1 lines 37-38)* the mirror area of the second controller on the basis of write operations issued by a host *(host 102, column 1 line 17)*. Beardsley discloses issuing a stop command to host applications to stop input/output to the primary device *(step 945, figure 9)*, which effectively stops processing by the primary controller.

Hubis and Beardsley are analogous art in that they deal with storage controllers maintaining access to data during controller failures. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Hubis's secondary controller to issue a stop command to applications communicating with the primary controller in the case of a failure, as taught by Beardsley.

Beardsley teaches that the motivation for doing so would have been to maintain data integrity during several types of primary and secondary subsystem errors *(column 8, lines 39-41)*. Therefore, it would have been obvious to combine Hubis' controllers with Beardsley's application stop command for the benefit of maintaining data integrity to obtain the invention as specified in claim 5.

21. As per **Claim 13**, Hubis and Beardsley disclose the storage control method according to Claim 12, further comprising

a step of disabling *(Beardsley, step 945, figure 9)* read/write processing to the mirror area of said second cache memory.

Claim Rejections - 35 USC ' 103 – Hubis and Rowson

22. **Claims 6 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis *(US Patent Number 6,321,298)* and in view of Rowson *("Interface-Based Design")*.

23. As per **Claim 6**, Hubis discloses the storage control apparatus according to Claim 1, wherein when said first controller receives a data write request for a page from said requesting apparatus, said first controller allocates a page in the read/write area of said first cache memory, acquires a storage page in the mirror area of said second cache memory referring to said first mirror management table, writes the write data from said requesting apparatus to the allocated page in the read/write area of said first cache memory, and copies the write data to the acquired page in the mirror area of said second cache memory. Hubis does not disclose the page instead being a plurality of pages, and writing the data of the next page to the next page allocated in the read/write area of said first cache memory during said copying.

Rowson discloses a data write request for a plurality of pages *(write-burst, section 5 paragraph 6 lines 1-3)*, and writing the data of the next page to the next page allocated in the read/write area of said first cache memory during said copying *(section 5, paragraph 7 lines 1-4)*.

Hubis and Rowson are analogous art in that they deal with caching write data. It would have been obvious at the time of the invention to design Hubis' cache system to handle write bursts and cache the write data while forwarding the write command to the drive, as taught by Rowson.

The motivation for doing so, as taught by Rowson, would be to minimize on-drive resources *(section 5, paragraph 6, line 3)* and to allow the drive to read data in an order optimized for disk scheduling *(section 5, paragraph 7, lines 10-12)*. Therefore, it would

have been obvious to combine Hubis's cache system with Rowson's write burst for the benefit of minimizing on drive resources and optimizing disk scheduling to obtain the invention as specified in claim 6.

24. As per **Claim 14**, Hubis and Rowson disclose the storage control method according to claim 9, further comprising

a step of writing *(Rowson, section 5, paragraph 7 lines 1-4)* the data of the next page to the next page allocated in the read/write area of said first cache memory during said copying when said one controller receives a data write request for a plurality of pages *(Rowson, write-burst, section 5 paragraph 6 lines 1-3)* from said requesting apparatus.

Claim Rejections - 35 USC ' 103 – Hubis and Li

25. **Claims 8 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis *(US Patent Number 6,321,298)* and in view of Li et al *("Evaluation of Memory System Extensions")*.

26. As per **Claim 8**, Hubis discloses the storage control apparatus according to claim 7, wherein said first control unit instructs *(Hubis, mirror cache write command, column 3 lines 57-58)* said first node channel circuit to execute the transfer of data of the page allocated in the read/write area of said first cache memory to the acquired page in the mirror area of said second cache memory, and performs said copying *(Hubis, column 3 lines 52-55)*. Hubis does not disclose the transfer being a DMA transfer.

Li discloses transferring data blocks between memories where the transfer is a DMA transfer *(lines 7-17, paragraph 3 of page 91)*.

Hubis and Li are analogous art in that they deal with transferring data between memory elements. It would have been obvious to one with ordinary skill in the art to

utilize DMA transfer when transferring data between the first and second controllers. The motivation for doing so would have been to allow the controller's control unit to do other useful work during the period of transfer *(lines 13-14, paragraph 3 of page 91)*. Therefore, it would have been obvious to combine the transfer of data used in Hubis with the DMA transfer described by Li for the benefit of increased processing time to obtain the invention as specified in claim 8.

27. As per **Claim 16**, Hubis and Li disclose the storage control method according to Claim 15, wherein said copying step comprises

a step of said first control unit instructing *(Hubis, mirror cache write command, column 3 lines 57-58)* said first node channel circuit to execute the DMA transfer *(Li, lines 7-17, paragraph 3 of page 91)* of the data of the page allocated in the read/write area of said first cache memory to the acquired page in the mirror area of said second cache memory and performing said copying *(Hubis, column 3 lines 52-55)*.

III. RELEVANT ART CITED BY THE EXAMINER

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Sicola et al. *(US Patent Number 5,974,506)* discloses a cache system with selectable cache modes that can partition the caches into two quadrants, one mirrored and one not.

b. Vishlitzky et al. *(US Patent Number 5,987,566)* discloses mirrored drive controllers with correspondence tables.

IV. CLOSING COMMENTS

a. STATUS OF CLAIMS IN THE APPLICATION

29. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(1). SUBJECT MATTER CONSIDERED ALLOWABLE

30. Claims 2 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record neither anticipates nor renders obvious the below recited combinations:

c. The primary reasons for allowance of Claims 2 and 10 in the instant application is the combination with the inclusion that:

said first and second controllers mutually notify the sizes of said first and second cache memories, allocate the mirror areas of said first and second cache memories according to the sizes of said first and second cache memories, and **create said first and second mirror management tables from said allocation**.

a(2). CLAIMS REJECTED IN THE APPLICATION

31. Per the instant office action, Claims 1, 3-9 and 12-17 have received an action on the merits and are subject of a non-final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 9:30-6:00.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

IMPORTANT NOTE

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sam Dillon
Examiner
Art Unit 2185

SAD

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100